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Application Note | Case Study | Technology Primer | **White Paper**

The Evolution of CMOS Imaging Technology

Innovations and improvements in CMOS imaging technology design and fabrication have allowed designers to overcome many traditional practical implementation issues. Although integrated circuit design is always a process of optimizing tradeoffs between limiters, CMOS imaging technology designers can now deliver products with performance that is truly compelling for machine vision applications. With these innovations and considerable time and investment, CMOS imaging technology has seen significant advancements and has increased in usage over competing CCD technology by original equipment manufacturers in the machine vision industry.

Choosing the most suitable camera for a specific machine vision application requires a delicate balancing of different attributes of the image sensor and camera with the needs of the machine vision system. The progress that has been made in CMOS technology over the past decade has made it the preferred technology for high speed inspection.

Three main attributes define the primary set of trade-offs for an area imaging device. The first set of attributes can be observed in imaging performance: image quality, maximum number of frames per second, and resolution. The second set of trade-off attributes is in the functionality of the camera or sensor, where competing features call for difficult decisions. Examples of these secondary trade-off attributes include features such as windowing and power consumption. Finally, there are feasibility trade-offs to be made which deal with cost, yield, reliability and other features related to the manufacturing of the imaging device.

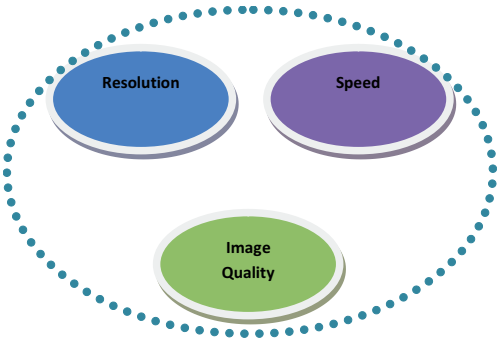

Figure 1: *CMOS Image Sensor Primary Trade-off*

Although in the past the image quality thresholds required the use of ILT CCD sensors (inter-line transfer CCD) in many applications, improvements in the design of CMOS sensors have led to better image quality and opened up new possibilities for much faster inspection systems with the desired image quality. Historically, CCD ILT technology was the dominant sensor technology for shuttered imaging. The first generation of CMOS technology entered the market offering only rolling shutter functionality, which precluded its use in most shuttered applications despite the opportunity for higher speed, lower power, and lower cost. Later on, the CMOS global shutter feature was introduced, solving the rolling shutter shortfall and allowing CMOS to be relevant to more users. Recent advances in the technology have vastly reduced the noise and improved signal to noise ratio (SNR) levels, in CMOS. CMOS technology surpasses what is possible in the CCD ILT, which was the last of the major performance hurdles. In high speed machine vision applications, CMOS meets or exceeds CCD ILT technology in functionality, performance, and cost.

The latest generations of CMOS imaging technology have diminished the trade-off between resolution and speed by using very high data throughput, made possible by very fast, high bandwidth analog to digital converters. The speed of these devices has challenged the boundaries of available data transmission standards such as CameraLink and has been the primary driving force behind the new high bandwidth CameraLink HS standard.

Advances in pixel structures, such as global shutter pixels, have already narrowed the gap between speed and image quality that has been an issue in high speed applications in the past. This technology is currently a de facto standard for any high end CMOS image sensor.

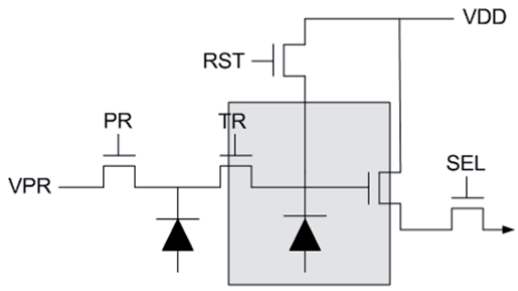

Figure 2: *Teledyne DALSA 5T Global Shutter CMOS Pixel, introduced in 1999*

Figure 3: *Global shutter, rolling shutter and image distortion*

Use of features such as Pinned Photodiode Technology (PPD) and optimized implantation techniques reduces the dark current and number of "hot pixels" as well as the noise and lag in an image. This has improved pixel signal to noise ratio. A lower noise floor means that new imagers can be used with less illumination at faster frame rates and still achieve the same image SNR as older, slower, noisier designs.

The benefits of the new CMOS imaging technology are not only confined to the CMOS imaging sensor. Advances in CMOS camera design techniques have also offered new possibilities in terms of imaging performance. For example, real time embedded processing in the camera compensates for non-idealities in the sensor, such as pixel response non-uniformity correction. This embedded processing in the camera also simplifies the vision system by performing processing that was traditionally done in a frame grabber, such as in-camera real-time flat field correction. Windowing capability and ability to change camera aspect ratio are other examples of how camera design, in conjunction with a CMOS image sensor, can provide additional capabilities to an end user.

Competing Factors at Play in CMOS Sensor Technology Evolution

When it comes to CMOS pixel structure design, there are a few fundamental competing factors that define the performance of the CMOS imaging sensor. Some of these trade-offs are fundamental and physical trade-offs and some are due to non-idealities in the silicon or in the implementation of the device. One of the main focuses of CMOS technology development in the past has been to overcome image artifacts. The user must pay close attention to the performance of a CMOS image sensor with regard to image artifacts arising in extreme situations or certain operation and lighting situations. This consideration heavily impacts a designer's decision when faced with design trade-offs. A sensor that has excellent combinations of specifications may prove to be unusable if it exhibits image artifacts.

Some of the major trade-off parameters are explained below:

A) Fill Factor
There is an inverse relationship between the number of transistors in a given pixel and its fill factor. Fill factor, the percentage of light sensitive area in a pixel, directly impacts the sensitivity of a sensor and S/N of the captured image. On the other hand, having more transistors in a pixel allows for additional features, such as global shutter and correlated double sampling (CDS) that enhance image quality.

B) Light Acceptance Angle
In order to minimize the impact of increased number of transistors per pixel, most CMOS image sensors use micro lenses. A micro-lens compensates for some of the lost real estate in a pixel due to increased number of transistors. However, micro-lenses reduce the "light acceptance angle" in a pixel. The use of micro-lenses somewhat improves the trade-off between the number of transistors in a pixel and image quality.

C) Pixel Charge Capacity (Qsat) and Maximum Exposure Level
Another major drawback of having more transistors in a pixel is reduced pixel charge capacity. In addition, a reduction in pixel size (increased resolution for the same size sensor), means less space for charge storage, which in turn results in lower pixel charge capacity. Reduced pixel capacity directly impacts the suitability of sensors for some applications. For example, many applications require the camera to differentiate between shades of grey in a bright image. In these applications, shot noise is the decisive factor and not the absolute noise floor. Since the signal to noise ratio in the shot noise limit scales with the square root of the captured photon signal, shot noise limited applications require high pixel storage capacity.
Higher pixel storage capacities also help to minimize the size and impact of several types of imager non-idealities such as blooming and parasitic image artifacts

D) Minimum Exposure Time and Resolution and Power
Minimum exposure time directly defines the maximum practical speed of the imaging device. A sensor that is not optimally designed can exhibit image artifacts at low exposure times while behaving normally at longer exposure times. In a CMOS sensor design, the minimum exposure time is determined by the signal propagation speed within the sensor. Voltage stabilization could be compromised by suboptimal signal routing schemes. This issue becomes more evident as the sensor resolution increases. On the other hand, an ability to clock a sensor fast enough to capture a really short exposure time will also lead to larger exposure control feed through artifacts as well as higher power consumption.

E) Minimum Achievable Noise Level
The minimum achievable noise level in a pixel is important in light-starved applications. Complex pixel circuitry and increased number of stages can negatively impact the noise floor of a sensor. Essential techniques, such as correlated double sampling (a must have feature in order to achieve equivalent or better noise figures as in CCD ILT devices), requires extra memory in the pixel architecture. This additional circuitry leaves less real estate in the pixel for light collection and signal storage and hence limits optical efficiency and maximum signal handling capacity.
There are a few schools of thought on how best to implement CDS in CMOS global shutter pixels. In general, "Charge Domain" techniques are superior to "Voltage Domain" techniques, but the former are more susceptible to shutter leakage.

F) Shutter Leakage
When a CMOS pixel is read out, the charges from the light sensitive area of the pixel are transferred to a storage area for subsequent charge to voltage conversion and data transfer. Since the storage area cannot be perfectly isolated from the imaging area of the pixel, unwanted signal may be collected in the storage node creating parasitic image artifacts. In order to reduce this charge spillage, the charge can be immediately converted into voltage and sampled. This technique, also known as "voltage domain" global shutter, requires use of extra capacitors. However, the down sides of this technique are increased noise floor level, relative to charge domain CDS as well as negative impact on almost all of the previously mentioned performance parameters.

An alternative approach to the "voltage domain" global shutter structure is a "Charge Domain" structure, where the transfer of the image into shielded area takes place in the "Charge Domain." This vastly reduces the complexity of the pixel but requires optimized implementation of the components within a pixel. To achieve a better trade-off scheme between global shutter and other performance parameters, CMOS fabrication process challenges must be met and overcome. Essentially, with this method, a reduced number of high quality elements in the pixel achieves the same result as a more complex pixel circuitry.

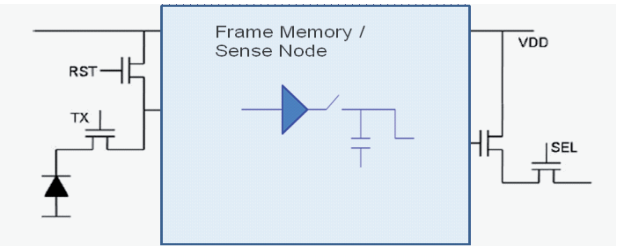

Figure 4: *Voltage Domain Global Shutter Architecture*

Conclusion
There are several competing factors at play in the CMOS imaging device design process. Some of the trade-offs are fundamental and related to the physics of operation of the device, while others are due to practical non idealities in the implementation of the design. A good CMOS imaging device design should consider all of these factors in order to come up with an optimal design. Future generations of CMOS technology will certainly continue to enhance the performance of imaging devices. Now users can benefit from both high resolution and high speed imaging devices that provide image quality that exceeds application requirements. Future generations of CMOS technology will defy today's limits with unprecedented combinations of imaging device attributes.

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